Adaptive Current Source Drivers for Efficiency Optimization of High-Frequency Synchronous Buck Converters

Zhiliang Zhang, *Member, IEEE*, Jizhen Fu, *Member, IEEE*, Yan-Fei Liu, *Senior Member, IEEE*, and Paresh C. Sen, *Life Fellow, IEEE*

***Abstract*—In this paper, the concept of the adaptive current source drivers (CSDs) is proposed for the high-frequency synchronous buck converters. Compared to the previous CSD circuits, the adaptive CSD can achieve adjustable drive current and drive voltage according to different load condition. The benefit is that higher drive current and voltage lead to lower switching loss and conduction loss when the load current increases. Therefore, the adaptive CSD is able to realize optimal design to reduce the switching loss, the gate drive loss, and the conduction loss in a wide load range. It should be noted that the adaptive concept is suitable for both the continuous and discontinuous CSDs regardless the drive circuit topologies. Through investigating the CSD circuits, one simple method to achieve the adaptive drive current based on the adaptive voltage is proposed. A 12 V input, 1.3 V output, and 1-MHz synchronous buck converter with the continuous and discontinuous CSDs was built, respectively, to verify the advantages of the proposed adaptive concept and efficiency improvement.**

***Index Terms*—Buck converter, current-source driver (CSD), power MOSFET, resonant gate driver, switching loss reduction, voltage regulator (VR), voltage regulator module (VRM).**

I. Introduction

RESONANT gate driver technique has been used in high current and low voltage applications such as voltage regulators (VRs). The resonant gate drivers are able to reduce the gate drive loss, i.e., CV^2 loss that occurs with the conventional voltage driver, at high-frequency operation (>1 MHz) [1]–[5]. Some self-oscillating resonant gate drivers (also called soft gating drivers) have been applied to very high frequency (VHF) dc/dc conversions to reduce high gate driving loss [6]–[9].

Manuscript received June 30, 2011; revised September 26, 2011; accepted October 28, 2011. Date of current version February 27, 2012. This work was supported by the Natural Science Foundation of China under Grant 51007036, the Delta Power Electronics Science and Education Development Fund under Grant DREG2010008, the Aviation Science Fund under Grant 2010ZC52037, and The Project of University Excellent Discipline, Jiangsu Province. Recommended for publication by Associate Editor M. Ponce-Silva.

Z. Zhang is with the Aero-Power Sci-Tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: zlzhang@nuaa.edu.cn).

J. Fu, Y.-F. Liu, and P. C. Sen are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada (e-mail: jizhen.fu@queensu.ca; yanfei.liu@queensu.ca; senp@post.queensu.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2011.2175453

Current source drivers (CSDs) have been proposed to reduce the excessive switching loss and gate driver loss for megahertz buck VRs. One of the most important benefits of the CSD technology is to achieve significant switching loss reduction of the power MOSFETs at the switching frequency of megahertz [10], [11]. The idea of the CSD circuits is to build a current source (CS) to charge and discharge the power MOSFET gate capacitance so that fast switching speed and reduced switching loss can be achieved. Based on this basic idea, different CSD topologies have been proposed. According to the current types of the CS inductor, the CSD topologies can be categorized as the continuous and discontinuous [12]–[16]. The continuous CSDs can use two drive MOSFETs with the complementary control to build a continuous current waveform in the CS inductor. Due to the continuous current, the drive switches are able to achieve zero-voltage-switching (ZVS), which is beneficial to megahertz operation. However, the CS inductor value is relatively high, and is typically around 1 μH at the switching frequency of 1 MHz. Furthermore, the inductor value and the drive current depend on the switching frequency in both dc–dc converters and Power Factor Correction (PFC) boost converters [17], [18].

In order to reduce the circulating loss in the driver circuit and reduce the CS inductor value, different discontinuous CSDs have been proposed [19]–[24]. In comparison, the discontinuous CSDs have much lower inductor value, which is around 20 nH. This significant inductance reduction leads to size and board area reduction. More importantly, the CS inductor value is independent of the switching frequency so that variable frequency control can be used with this type of CSDs. Nevertheless, to build a discontinuous current, more drive switches are generally needed and sophisticated control timing is also required.

For the CSD technology, high drive current normally leads to lower switching loss. A stronger drive current is desired to reduce the switching loss further when the power MOSFET carries higher current. Nevertheless, higher drive current also results in higher circulating loss [15]–[19]. However, the present CSD circuits normally use constant drive current and voltage. For the control FETs, stronger drive current means fast switching speed and lower switching loss, but results in higher drive circuit loss. This leads to a tradeoff between the switching loss reduction and gate drive loss. For the sync FETs, stronger drive current means fast switching speed and then lower body diode loss, but results in higher gate drive loss. This leads to a tradeoff between the body diode loss and gate drive loss. However, constant drive current and voltage limit the optimal operating conditions of the

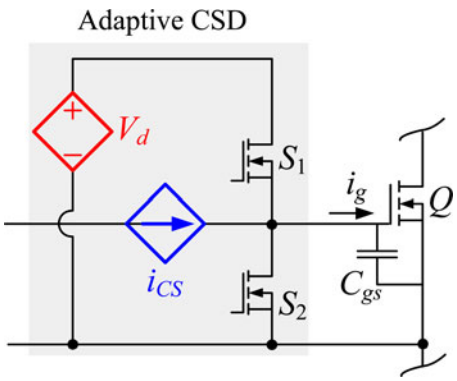

Fig. 1. Proposed adaptive CSD concept.

loss reduction. To achieve high-efficiency curves through wide load range becomes an important topic for high-frequency VRs. High gate drive current and voltage are beneficial to the nominal load conditions, but hurt light load efficiency, which is of great importance for buck VRs.

Therefore, the adaptive drive current would be beneficial to improve the performance of the CSDs and helps to achieve optimal design of the switching loss reduction and gate drive loss reduction. The objective of this paper is to propose the adaptive CSD concept to improve the performance of the CSD technique. The proposed adaptive CSD could achieve different optimal drive current depending on the drain current in the power MOSFETs, or the load conditions and input voltage. Section II presents the proposed adaptive concept for the CSDs. Section III presents the adaptive continuous CSDs. Section IV presents the adaptive discontinuous CSDs. Section V is the implementation of the adaptive CSDs. Section VI contains the experimental results and discussion. Section VII is the conclusion.

II. Proposed Adaptive CSD Concept for High-Frequency MOSFETs

The proposed adaptive CSD concept is illustrated in Fig. 1 This can be regarded as a general structure for the adaptive CSDs. In Fig. 1, S_1 and S_2 form a totem structure to provide a low impedance path for the gate terminal of the power MOSFET Q either during the turn-on condition or turn-off condition. The adaptive parameters are defined as follows: 1) V_d is a controlled voltage source as the CSD adaptive drive voltage from drive supply voltage V_c. It can be controlled with the variables in the power circuits such as load current, drain current of the switching devices and input voltage, etc. Higher drive voltage results in lower $R_{\mathrm{DS(on)}}$ and thus lower conduction losses, but increases drive losses. 2) i_{CS} is a controlled current source as the drive current for Q. It can also be controlled with the loads, drain current, and voltage in the power circuit. Higher drive current reduces the switching loss but increases the gate drive loss.

Compared to other CSD circuits, the controllable drive current and drive voltage is beneficial to the optimal design between the switching loss and drive loss during the wide range operation of the main power MOSFETs. This concept can be extended to most of the CSD circuit topologies. In this paper, two basic

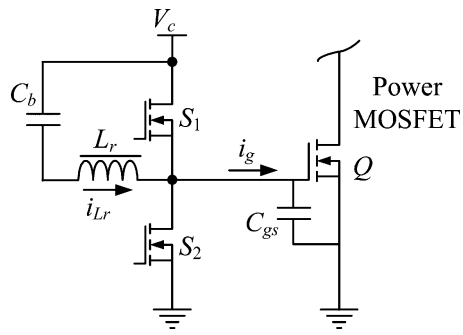

Fig. 2. Continuous CSD.

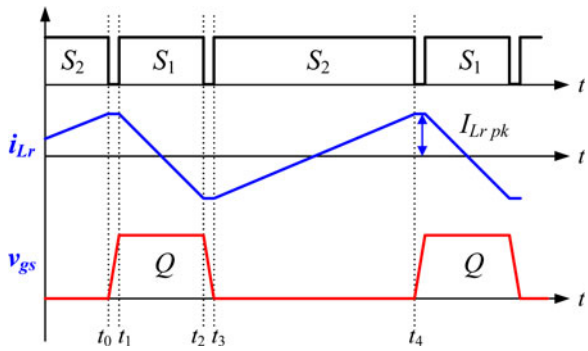

Fig. 3. Key waveforms of the continuous CSD.

structures of the continuous CSD and discontinuous CSD are investigated to achieve this adaptive control.

III. Adaptive Continuous CSD

A. Circuit Description

Fig. 2 shows the continuous CSD circuit, which is the half-bridge topology and consists of two drive MOSFETs S_1 and S_2. V_c is the drive voltage, L_r is the current source inductor, and C_b is the blocking capacitor. The basic idea of the continuous CSD is using a small inductance to build a strong current source to expedite the switching speed of the power MOSFET while recovering partial of the gate energy with reduced circulating losses [5], [15], [16].

Fig. 3 gives the key waveforms. S_1 and S_2 are switched out of phase with the complementary control to achieve ZVS. The inductor current is continuous and triangle. The MOSFET Q is charged or discharged by approximately constant current I_{Lrpk}, which is provided by the CS inductor L_r during $[t_0, t_1]$ and $[t_2, t_3]$ as shown in Fig. 3, respectively. When the gate is fully charged to V_c, the drive transistor S_1 is turned ON so that it provides a low impedance path to the gate voltage source. At the same time, i_{Lr} raises linearly. The turn-off transition is initiated by turning S_1 OFF. When the gate capacitance is fully discharged, S_2 is turned ON so that it shunts the gate and the source of the power MOSFET. S_1 and S_2 are turned ON and OFF at zero voltage.

The major advantage of this approach is simplicity since only one additional inductor and a capacitor are added compared to a conventional gate drive circuit. More importantly, the power

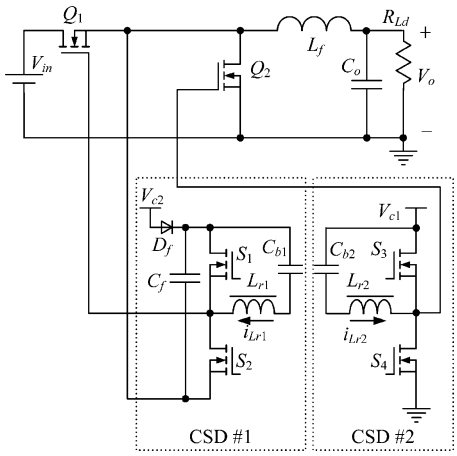

Fig. 4. Buck VR with the continuous CSD.

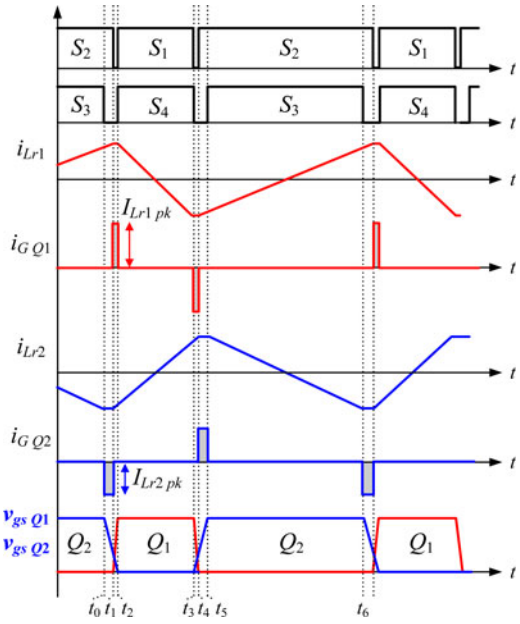

Fig. 5. Key waveforms of the continuous CSD.

MOSFET has fast switching speed because the current to charge and discharge MOSFET's input capacitor is almost constant. In addition, the drive circuit has good *Cdv/dt* immunity because the MOSFET gate-to-source voltage is clamped at either V_c (turn-on status) or zero (turn-off status).

B. Synchronous Buck Converter With the Continuous CSD

Fig. 4 shows the continuous CSD applied to the synchronous buck converter, where Q_1 is the control FET and Q_2 is the sync FET. V_{c1} and V_{c2} are the drive supply voltage. In Fig. 4, there are two sets of the drive circuits (CSD #1 and CSD #2) and each of them has the structure of the half-bridge topology, consisting of drive MOSFETs S_1 and S_2 and S_3 and S_4, respectively. Fig. 5 gives the key waveforms. CSD #1 can also be regarded as a level-shift version of CSD #2 [15].

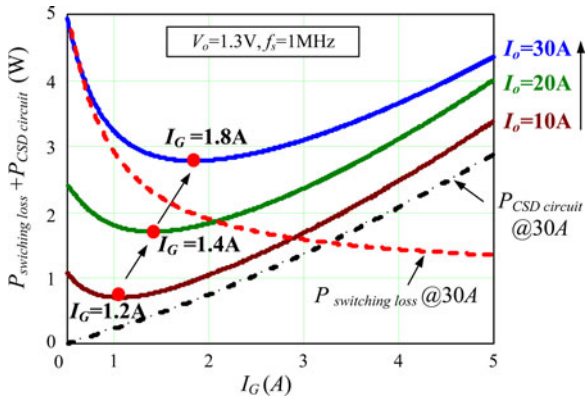

Fig. 6. Optimization curves for the control FET Q_1 with different current: power loss versus gate current.

C. Optimal Design and Adaptive Control With the Continuous CSD

For a given application, in order to achieve fast switching speed, the gate drive current should be chosen properly. The design tradeoff is between switching speed, which translates into reduced switching loss and gate drive loss. In order to find the optimal design point, the object function adding the switching loss and the CSD circuit loss together is used. The object function is a U-shape curve as function of the drive current I_G, and the optimization solution is simply located at the lowest point of the curve. Based on the above idea, Fig. 6 illustrates the optimal curve for the continuous CSDs with different load current, which includes the switching loss $P_{\text{switching loss}}$, the CSD circuit loss $P_{\text{CSD circuit}}$, and the objective function $F(I_G) = P_{\text{switching loss}} + P_{\text{CSD circuit}}$ as function of the gate drive current I_G. The specifications of the buck converter are: $V_{\text{in}} = 12$ V; $V_o = 1.3$ V; $I_o = 30$ A; $V_c = 5$ V; $f_s = 1$ MHz; control FET Q_1: Si7386DP; Q_2: IRF6691; and $L_f = 330$ nH.

From Fig. 6, at 30 A and with the increase of I_G, the switching loss $P_{\text{switching loss}}$ keeps reducing due to stronger drive current while the CSD circuit loss $P_{\text{CSD circuit}}$ keeps increasing due to high circulating current. The summation of these two, i.e., $F(I_G)$, is a U-shaped curve, and therefore, the optimization solution can be found at the lowest point of the curve. At the load current of 30 A, the optimal drive current I_G is chosen as 1.8 A for the continuous CSD. However, when the load changes, the optimal point will also change depending on the switching loss associated with the drain current in the MOSFET. It is interesting to note that when the load current increase from 10 to 30 A, the optimal drive current increases accordingly from 1.2 to 1.8 A. This means that higher drive current leads to lower switching losses. So the desired CSD current should be able to adjust adaptively as the load current increase. Although the optimal design curves are calculated from the above-mentioned specifications, it should be pointed that the trend of the optimal design curves are independent with the specification used, and the physical meaning of adaptive concept and design method is general.

Similarly, Fig. 7 gives the optimal curves for the Sync FET according to the load conditions, where P_{bodyloss} is the body

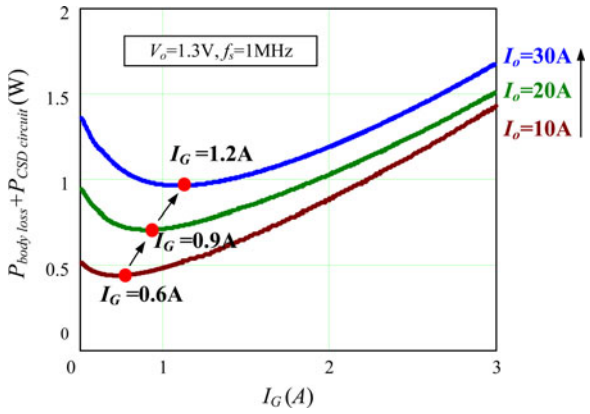

Fig. 7. Optimization curves for the sync FET Q_2: power loss versus gate current.

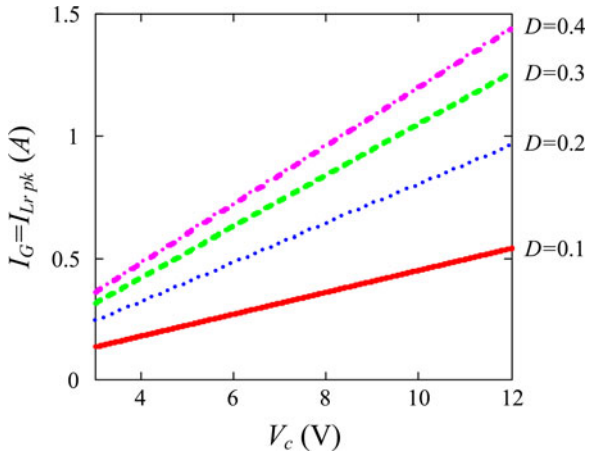

Fig. 8. CS current as function of the drive supply voltage with different duty cycles: continuous.

diode loss, $P_{\mathrm{CSD\ circuit}}$ is the CSD circuit loss, and $F(I_G) = P_{\mathrm{bodyloss}}+P_{\mathrm{CSD\ circuit}}$ is the objective function. The sync FET Q_2 operates with ZVS since its output capacitance is discharged to zero voltage before it turns on. Therefore, for the sync FET, the optimal design involves a tradeoff between body diode conduction loss and gate drive loss. When the load current increases from 10 to 30 A, the optimal drive current increases from 0.6 to 1.2 A, accordingly. High drive current leads to lower body diode conduction and body diode loss.

For the continuous CSD, the peak value of the CS inductor current is the drive current, which is

$$I_G = I_{Lrpk} = \frac{V_c \cdot D \cdot (1-D)}{2 \cdot L_r \cdot f_s} \tag{1}$$

where V_c is the drive supply voltage, D is the duty cycle, and L_r is the CS inductor.

Fig. 8 shows the drive current as function of the drive voltage with different duty cycles. For the continuous CSD, with the same duty cycle, the CS inductor current, i.e., the drive current, increases linearly when the drive voltage increases. Therefore, the adaptive drive current control of the CSDs can be translated into the adaptive drive voltage control. In this way, the drive voltage can be controlled according to different load conditions, so that higher drive current can be achieved to the optimal performance of switching loss reduction. Another important advantage of the adaptive drive voltage control is that higher gate drive voltage leads to lower $R_{\mathrm{DS(on)}}$ and thus lower conduction loss. This means in addition to the switching loss reduction with the adaptive drive current, the conduction loss can be reduced with the adaptive drive voltage control at the same time.

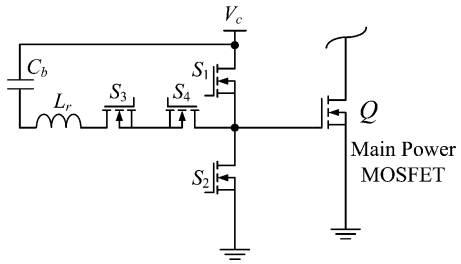

Fig. 9. Discontinuous CSD.

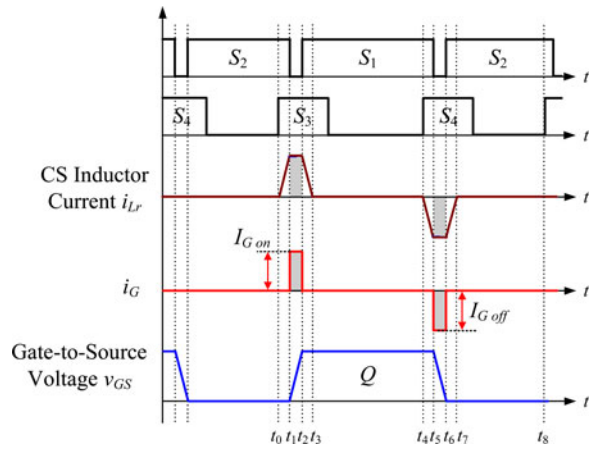

Fig. 10. Key waveforms of the discontinuous CSD.

IV. Adaptive Discontinuous CSDs

A. Circuit Description

Fig. 9 shows the discontinuous CSD circuit and Fig. 10 gives the key waveforms. In order to achieve discontinuous inductor current, S_3 and S_4 are inserted in series with the L_r and form a bidirectional switch, so that the current in the inductor can be controlled as desired. The key to this CSD is to control the driver switches to generate discontinuous inductor current waveforms enabling the peak portion of the inductor current to be used to charge and discharge the power MOSFET gate capacitance as a nearly constant current source [19], [22].

Compared to the continuous CSD, the advantage of the discontinuous CSD is very low inductance value owing to the discontinuous current operation of the CS inductor. At the same time, the gate drive current no longer depends on the duty cycle and switching frequency. This makes this type of CSDs suitable to wide range operation. In addition, the fast switching speed to reduce the switching loss and gate energy recovery can also be achieved.

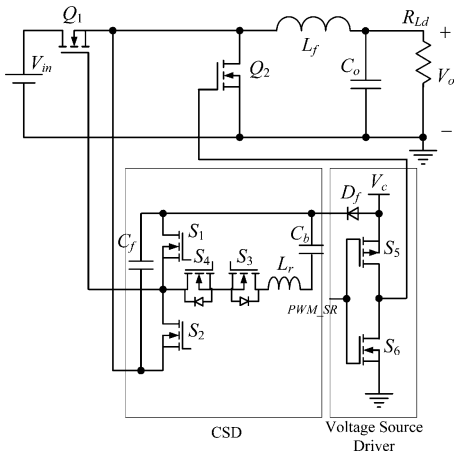

Fig. 11. Buck converter with the discontinuous CSD. (a) Power loss versus gate current. (b) Gate drive current versus load current.

B. Synchronous Buck Converter With the Discontinuous CSD

Fig. 11 shows the proposed hybrid gate drive scheme for a buck converter. As we know, for a buck VR, the dominant loss is the switching loss. Therefore, for the control FET Q_1, the proposed high side CSD is used to achieve the switching loss reduction. For the Synchronous Rectifier (SR) Q_2, the conventional voltage source driver is used for low cost and simplicity. Pulse width modulation_ saturable reactor (SR) is the signal fed into the voltage source driver. The details of the operation and optimal design of the buck converter with the discontinuous CSD have been addressed in [22].

C. Optimal Design and Adaptive Control With the Discontinuous CSD

Fig. 12(a) shows the power loss as the function of the adaptive drive current and Fig. 12(b) shows the adaptive gate current with different load current. As the load current increases from 10 to 30 A, the optimal drive current increases from 1.8 to 2.8 A, accordingly. The switching current in the control FET increases as the load current increases, which leads the switching loss to increase accordingly. Therefore, the switching time needs to be minimized with stronger gate drive current to reduce the switching loss. This results in the relationship between the gate drive current and output current as shown in Fig. 12(a). It should be also noted that at the same load current of 30 A, the optimal drive current I_G is chosen as 2.8 A (see Fig. 12) for the discontinuous CSD while the optimal drive current is 1.2 A (see Fig. 7) for the continuous one. This is because the discontinuous CSD has lower drive circulating loss over the continuous one, which helps to achieve high drive current.

For the discontinuous CSD, referring to Fig. 10, the precharge current to turn ON the power MOSFET is

$$I_{G\,\mathrm{on}} = \frac{V_C}{2L_r} \cdot \Delta t_{10} \tag{2}$$

where V_C is the drive voltage and Δt_{10} is the precharge interval from t_0 to t_1.

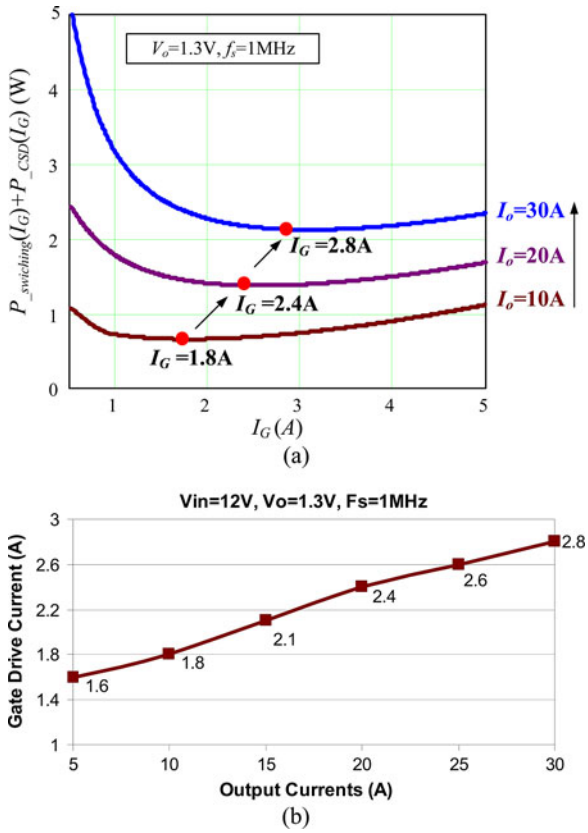

Fig. 12. Optimization curves for the control FET Q_1: discontinuous.

Similarly, the precharge current to turn OFF the power MOSFET is

$$I_{G\,\mathrm{off}} = \frac{V_{Cb}}{L_r} \cdot \Delta t_{54} = \frac{V_C}{2L_r} \cdot \Delta t_{54} \tag{3}$$

where V_{Cb} is the DC voltage across the capacitor and Δt_{54} is the precharge interval from t_4 to t_5.

From (3), it can be observed that the drive current only depends on the drive voltage V_c and precharge time with the certain CS inductance. Fig. 13 shows the drive current as function of the drive voltage with different drive voltage. Similar to the continuous CSD, the drive current also increases linearly when the drive voltage increases. So the adaptive drive voltage also leads to the adaptive drive current. More importantly, for the discontinuous CSD, the drive current is independent with the duty cycles. This makes the discontinuous CSDs suitable for variable fast duty cycle controls.

V. Implementation of the Adaptive Drive Voltage for the CSDs

As discussed in Section IV, for both of the continuous and discontinuous CSDs, the drive current is proportional to the drive voltage. One method to build the adaptive drive current is to adjust the drive voltage adaptively according to the load current, or input voltage, etc.

Normally, to achieve adaptive voltage function, a lower power switching converter or a linear regulator can be used. The

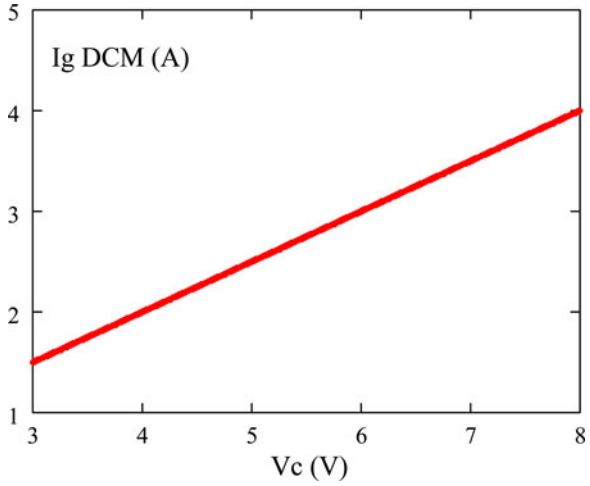

Fig. 13. CS current as function of the drive supply voltage: discontinuous. (a) Circuitry of the adaptive control voltage $V_{\rm REF}$. (b) Linear regulator with adaptive control voltage.

switching converters have higher efficiency over the linear regulators. However, it generally needs output filter inductors, such as buck converters, which are difficult to be integrated into a drive chip. The advantage of the linear regulator is that no inductors are required. This makes the integration of the linear regulator become achievable. As an example, UCC27222 from Texas Instrument (TI) have an integrated linear regulator to achieve desired voltage for its drive circuitry.

Fig. 14 gives schematic of the adaptive control circuit using the basic linear regulator. The advantage of using the linear regulator is that compact structure and fast voltage changes rate. Fig. 15 gives the simulated waveforms using SPICE software. In Fig. 14(a), $R_{\rm sens}$ is the sensor resistor and the voltage across $R_{\rm sens}$ is proportional to the load current. This voltage is sent into the amplifying stage. Three operational amplifiers are used to amplify the input signal linearly. The first and third amplifiers are used as inverting amplifiers and the second amplifier is used to realize the addition of the amplified input signal and the bias voltage V_a. The relationship between the reference voltage and the output current is

$$V_{\rm REF} = \frac{R_{\rm sens}R_2R_6R_9}{R_1R_5R_8}I_{\rm o} + \frac{R_6R_9}{R_5R_8}V_a. \qquad (4)$$

Fig. 14(b) shows the basic linear regulator with the reference voltage $V_{\rm REF}$. The output voltage V_d of the linear regulator is used to supply the CSD drive circuitry. When $V_{\rm REF}$ varies according to the load current I_o from (4), the output voltage V_d changes adaptively.

Using linear regulator to achieve adaptive voltage control results in additional loss and the efficiency of the linear regulator is $\eta = V_d/V_c$. The loss of the linear regulator is $P_{Vc}\cdot(1-\eta)$, where P_{Vc} is the drive supply power. However, the total loss reduction of the switching loss, the conduction loss, and the gate drive loss from the main power stage weighs much higher than the introduced loss with linear regulator. Therefore, the overall loss reduction improves the converter efficiency effectively in a wide load range.

VI. Experimental Results and Discussion

In order to verify the proposed adaptive concept, the synchronous buck converters with the continuous and discontinuous CSDs were implemented. The specifications of the buck converter prototype are as follows: input voltage $V_{\rm in} = 12$ V; output voltage $V_o = 1.3$ V; output current $I_o = 30$ A; switching frequency $f_s = 1$ MHz. The PCB is six-layer with 4 oz copper. The components used in the circuit are listed as follows—Q_1: Si7386DP; Q_2: IRF6691; output filter inductance: $L_f = 330$ nH (IHLP-5050CE-01, Vishay); for the continuous CSD, $L_r = 1$ μH; for the discontinuous CSD, $L_r = 22$ nH; drive switches S_1–S_4: FDN335.

Fig. 16 shows the gate drive signals v_{GSQ1} (control FET) and the CS inductor current i_{Lr} with the continuous CSD. The inductor current is triangle waveform and its peak current value is 1.8 A, which is the optimized value for the switching loss reduction.

Fig. 17 shows the inductor current i_{Lr} with the discontinuous CSD at the load current of 30 A. Its peak current value is 2.8 A, which is the optimized value of the CSD drive current at 8-V gate voltage. After the precharge time, the inductor current continues to ramp up while charging the gate capacitance of the control FET (Si7386DP) during the turn-on interval. During this interval, the average drive current is approximately 2.6 A. After the control FET turns ON, the inductor current ramps back down to zero while the inductor energy is returned to drive voltage source.

Fig. 18 shows the gate drive signals v_{GSQ1} (control FET) and v_{GSQ2} (Sync FET). It is observed that v_{GSQ1} is smooth since the miller charge is removed fast by the constant inductor drive current. Moreover, the total rise time and fall time of v_{GSQ1} is less than 15 ns, which means that fast switching speed is achieved. The dead time between two drive voltages is fixed to avoid shoot through and is minimized to reduce the SR body diode conduction loss.

A benchmark of a synchronous buck converter with the conventional gate driver was also built. The Predictive Gate Drive UCC 27222 from TI was used as the conventional voltage driver. Fig. 19 shows the measured efficiency comparison between the continuous CSDs with and without the adaptive voltage at 1.3 V output. It is observed that at 5 A, the efficiency is improved from 79.1% to 85.7% (an improvement of 6.6%) with the drive voltage of 4 V. The loss of the linear regulator is 0.13 W. At 10 A, the efficiency is improved from 86.2% to 88.4% (an improvement of 2.2%) with the drive voltage of 5 V. The loss of the linear regulator is 0.22 W. It should be also noted that the CSDs improve the efficiency effectively in full load range over the conventional driver.

Fig. 20 shows the measured efficiency comparison between the discontinuous CSDs with and without the adaptive voltage at 1.3 V output. It is observed that at 5 A, the efficiency is improved from 80.6% to 86.1% (an improvement of 5.5%) with the drive voltage of 4 V. At 10 A, the efficiency is improved from 85.6% to 88.6% (an improvement of 3%) with the drive voltage of 5 V. It should be also noted that the CSDs improve the efficiency effectively in the full load range over the conventional driver. The

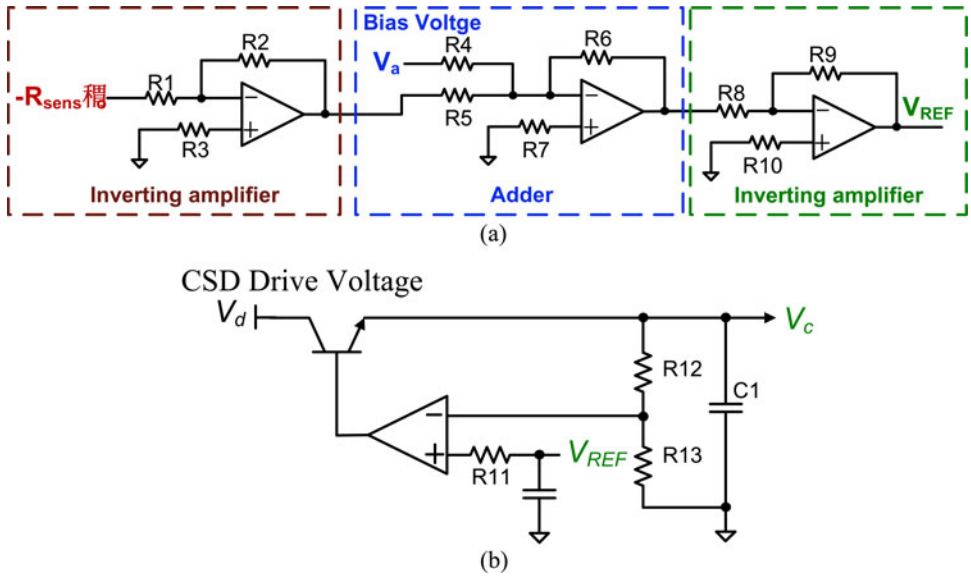

Fig. 14. Adaptive drive voltage circuit using the basic linear regulator.

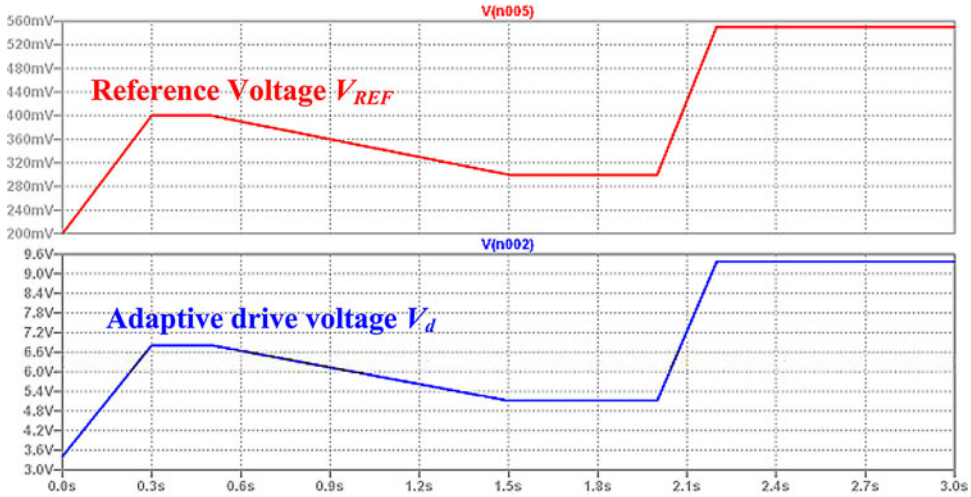

Fig. 15. Simulated waveforms of adaptive drive voltage.

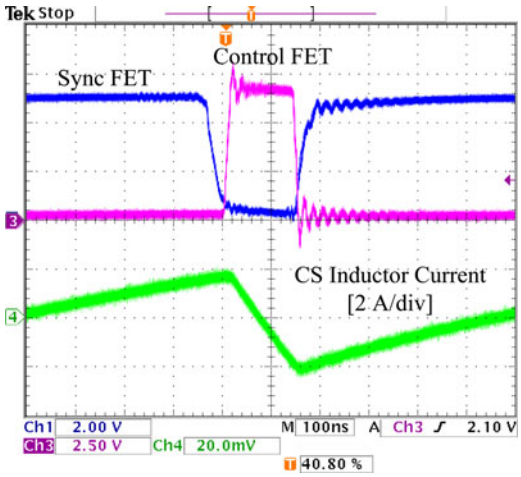

Fig. 16. Gate drive voltage and CS inductor current: continuous.

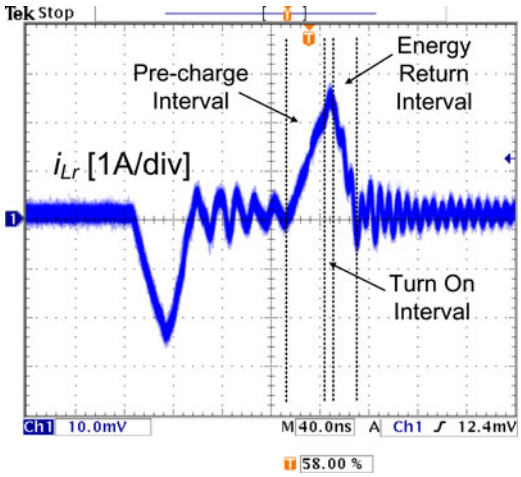

Fig. 17. Inductor current at 1 MHz: discontinuous.

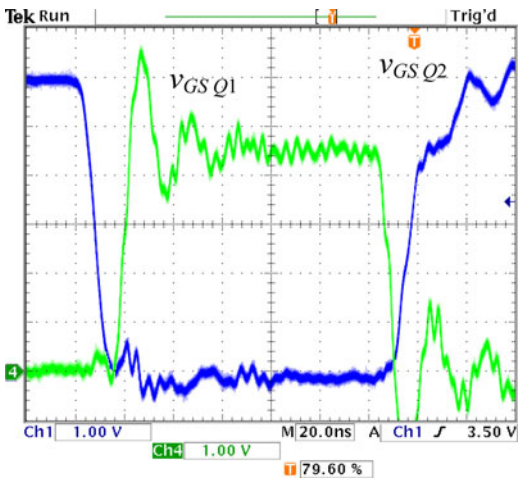

Fig. 18. Gate signals v_{GSQ1} (control FET) and v_{GSQ2} (Sync FET).

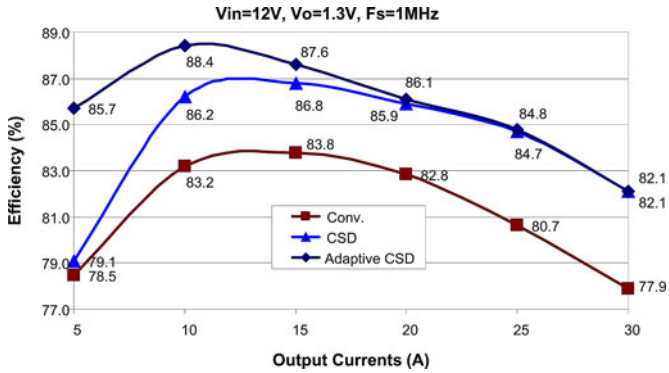

Fig. 19. Efficiency comparison: continuous.

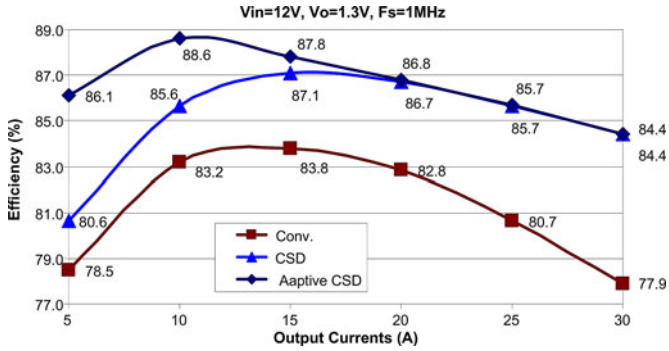

Fig. 20. Efficiency comparison: discontinuous.

adaptive CSD achieves higher efficiency improvements during lower load range since the switching losses that occur with light load reduces greatly.

VII. Conclusion

Constant drive current and drive voltage are presently accepted for the CSD circuits to reduce the switching loss and gate drive loss. However, stronger drive current is normally desired to reduce the switching loss further when the power MOSFET carries higher current. In a synchronous buck converter, for the control FET, the design tradeoff is between the switching loss and gate drive loss, while for the sync FETs, it is between the body diode loss and gate drive loss. However, constant drive current and voltage limit the optimal operating conditions of the loss reduction.

In this paper, the concept of the adaptive CSDs is proposed for the high-frequency synchronous buck converters. Compared to the previous CSD circuits, the adaptive drive current and drive voltage can be achieved to optimize the switching loss reduction and the drive loss reduction at different load current. It should be noted that the adaptive concept is suitable for both the continuous and discontinuous CSDs regardless the drive circuit topologies. Through investigating the CSD circuits, one simple method to achieve the adaptive drive current based on the adaptive voltage is proposed. The linear regulator can be used to achieve the function of the adaptive voltage and drive current in a cost-effective manner. A 12 V input, 1.3 V output, and 1-MHz synchronous buck converter was built to verify the advantages of the proposed adaptive CSDs. For the continuous CSD, at 1.3 V output, the adaptive CSD improves the efficiency from 79.1% (without adaptive control) to 85.7% (an improvement of 6.6%) at 5 A, and at 10 A, from 86.2% to 88.4% (an improvement of 2.2%). Similar efficiency improvements are achieved for the discontinuous CSDs.

References

[1] K. Jin, M. Xu, Y. Sun, D. Sterk, and F. C. Lee, "Evaluation of self-driven schemes for a 12-V self-driven voltage regulator," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2314–2322, Oct. 2009.

[2] Z. Zhang, E. Meyer, Y. F. Liu, and P. C. Sen, "A 1-MHz, 12-V ZVS non-isolated full-bridge VRM with gate energy recovery," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 624–636, Mar. 2010.

[3] Z. Zhang, J. Zhen, Y. F. Liu, and P. C. Sen, "A non-isolated ZVS self-driven current tripler topology for low voltage and high current applications," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 512–522, Feb. 2010.

[4] Q. Li and P. Wolfs, "The power loss optimization of a current fed ZVS two-inductor boost converter with a resonant transition gate drive," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1253–1263, Sep. 2006.

[5] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, 1991, pp. 527–532.

[6] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Effects of parasitic components in high-frequency resonant drivers for synchronous rectification MOSFETs," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2082–2092, Jul. 2008.

[7] J. R. Warren, K. A. Rosowski, and D. J. Perreault, "Transistor selection and design of a VHF DC-DC power converter," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 27–37, Jan. 2008.

[8] M. Swamy, T. J. Kume, and N. Takada, "An efficient resonant gate drive scheme for high frequency applications," in *Proc. IEEE Energy Convers. Conf. Expo. (ECCE)*, 2011, pp. 1985–1963.

[9] T. M. Andersen, S. K. Christensen, A. Knott, and M. A. E. Andersen, "A VHF class E DC-DC converter with self-oscillating gate driver," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2011, pp. 885–891.

[10] Z. Yang, S. Ye, and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1311–1320, Jul. 2007.

[11] W. Eberle, Z. Zhang, Y. F. Liu, and P. C. Sen, "A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 678–691, Mar. 2008.

[12] K. Yao and F. C. Lee, "A novel resonant gate driver for high frequency synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 180–186, Mar. 2002.

[13] Y. Ren, M. Xu, Y. Meng, and F. C. Lee, "12 V VR efficiency improvement based on two-stage approach and a novel gate driver," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, 2005, pp. 2635–2641.

[14] Z. Yang, S. Ye, and Y. F. Liu, "New dual channel resonant gate drive circuit for low gate drive loss and low switching Loss," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1574–1583, May 2008.

[15] Z. Zhang, W. Eberle, P. Lin, Y. F. Liu, and P. C. Sen, "A 1-MHz high efficiency 12 V buck voltage regulator with a new current-source gate driver," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2817–2827, Nov. 2008.
[16] Z. Zhang, W. Eberle, Z. Yang, Y. F. Liu, and P. C. Sen, "Optimal design of resonant gate driver for buck converter based on a new analytical loss model," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 653–666, Mar. 2008.
[17] Z. Zhang, P. Xu, and Y. F. Liu, "Adaptive current source drivers for MHz power factor correction," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2011, pp. 161–166.
[18] P. Xu, Z. Zhang, Y. F. Liu, and P. C. Sen, "Adaptive discontinuous current source driver to achieve switching loss reduction for MHz PFC applications," in *Proc. IEEE Energy Convers. Conf. Expo. (ECCE)*, 2011, pp. 1346–1352.
[19] S. Pan and P. K. Jain, "A new pulse resonant MOSFET gate driver with efficient energy recovery," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, 2006, pp. 1–5.
[20] X. Zhou, Z. Liang, and A. Huang, "A new resonant gate driver for switching loss reduction o f high side switch in buck converter," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2010, pp. 1477–1481.
[21] H. Fujita, "A resonant gate-drive circuit capable of high-frequency and high-efficiency operation," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 962–969, Apr. 2010.
[22] Z. Zhang, J. Fu, Y. F. Liu, and P. C. Sen, "Discontinuous current source drivers for high frequency power MOSFETs," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1863–1876, Jul. 2010.
[23] Z. Zhang, J. Zhen, Y. F. Liu, and P. C. Sen, "Switching loss analysis considering parasitic loop inductance with current source drivers for buck converters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1815–1819, Jul. 2011.
[24] J. Fu, Z. Zhang, Y. F. Liu, P. C. Sen, and L. Ge, "A new high efficiency current source driver with bipolar gate voltage," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 985–997, Feb. 2012.

Zhiliang Zhang (S'03–M'09) received the B.Sc. and M.Sc. degrees in electrical and automation engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2002 and 2005, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2009.

Since June, 2009, he has been an Associate Professor with Aero-Power Sci-Tech Center, Nanjing University of Aeronautics and Astronautics. He was a Design Engineering Intern at Burlington Design Center, VT, Linear Technology Corporation, from June to September 2007. His research interests include high-frequency dc–dc converters, power integrated circuit, digital control techniques for power electronics, and renewable energy conversion system.

Dr. Zhang was a recipient of the Graduate Scholarship through Lite-On Technology Corporation in 2004 and a winner of "United Technologies Corporation Rong Hong Endowment" in 1999.

Jizhen Fu (S'08–M'10) received the B.Eng. degree from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2008, and Master of Applied Science degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2010.

From June 2010 to June 2011, he was a Power MOSFET Applications Engineer with International Rectifier (IR), Los Angeles, CA. Since June 2011, he has been the System Design Engineer with mainly focusing on the cutting-edge IR gallium nitride (GaN) device. His research interests include novel gate drive techniques for next-generation voltage regulators, very high frequency resonant converter, digital control, and integrated circuits.

Mr. Fu has received several travel grants both from IEEE Power Electronics Society (PELS) and Power Source Manufactures Association (PSMA) to present the papers in conferences. He is also the recipient of the Presenter Award in the IEEE Applied Power Electronics Conference and Exposition (APEC), Palm Spring, 2010.

Yan-Fei Liu (M'94–SM'97) received the B.Sc. and M.Sc. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1984 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada in 1994.

From February 1994 to July 1999, he was a Technical Advisor with the Advanced Power System Division, Astec (formerly Nortel Networks), where he was engaged in high-quality design, new products, and technology development. Since 1999, he joined Queen's University. Currently, he is a Professor in the Department of Electrical and Computer Engineering, Queen's University. His research interests include digital control technologies for dc-dc switching converter and ac-dc converter with power factor correction, current source MOSFET drive technology, topologies and control for voltage regulator application, electromagnetic interference filter design methodologies for switching converters, topologies and controls for high switching frequency, low switching loss converters, modeling, and analysis of core loss and copper loss for high-frequency planar magnetics, and large signal modeling of switching converters.

Dr. Liu has been an Associate Editor on IEEE TRANSACTIONS ON POWER ELECTRONICS since 2001. He is a technical program chair for ECCE 2011. He is a chair of the Technical Committee on Power Conversion Systems and Components of IEEE Power Electronics Society. He also served as technical program chair for the 2010 International Workshop of Power Supply on Chip held in Cork Ireland, as well as a technical program vice chair for ECCE 2010. He holds 16 US patents and has published more than 100 technical papers in IEEE Transactions and Conferences. He was a recipient of the 2001 Premiere's Research Excellence Award in Ontario, Canada and the 1997 Award in Excellence in Technology from Nortel Networks.

Paresh C. Sen (M'67–SM'74–F'89–LF'03) was born in Chittagong, Bangladesh. He received the B.Sc. (with honors in physics) and M.Sc. (Tech.) degrees in applied physics from the University of Calcutta, Kolkata, India, in 1958 and 1961, respectively, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1965 and 1967, respectively.

He is currently an Emeritus Professor of Electrical and Computer Engineering at Queen's University, Kingston, ON, Canada. He has published more than 160 research papers in the area of power electronics and drives. He is the author of two internationally acclaimed textbooks: *Principles of Electric Machines and Power Electronics* (New York: Wiley, 1989, 2nd ed., 1997) and *Thyristor DC Drives* (New York: Wiley, 1981). His research interests include power electronics, electric drive systems, switching power supplies, power factor correction circuits, modern control techniques for high-performance drive systems, and applications of fuzzy logic control in power electronics and drive systems.Dr. Sen is the recipient of the IEEE Canada Outstanding Engineering Educator Award in 2006 for his outstanding contributions over four decades as an author, teacher, supervisor, researcher, and consultant. He received the Prize Paper Award from the Industrial Drives Committee for technical excellence at the IEEE Industry Applications Society (IAS) Annual Meeting in 1986. He has served as an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS (1975–1982) and as the Chairman of the Technical Committees on Power Electronics (1979–1980) and Energy Systems (1980–1982) of the IEEE Industrial Electronics Society. He served as a Natural Science and Engineering Research Council of Canada (NSERC) Scientific Liaison Officer evaluating University-Industry coordinated projects (1994–1999).